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INTERNATIONAL
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**CEI
IEC**

60841

Première édition
First edition
1988-03

**Enregistrement sonore –
Système codeur et décodeur à modulation
par impulsions codées (MIC)**

**Audio recording –
PCM encoder / decoder system**



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Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**AUDIO RECORDING –
PCM ENCODER/DECODER SYSTEM**

FOREWORD

- 1) The formal decisions or agreements of the IEC on technical matters, prepared by Technical Committees on which all the National Committees having a special interest therein are represented, express, as nearly as possible, an international consensus of opinion on the subjects dealt with.
- 2) They have the form of recommendations for international use and they are accepted by the National Committees in that sense.
- 3) In order to promote international unification, the IEC expresses the wish that all National Committees should adopt the text of the IEC recommendation for their national rules in so far as national conditions will permit. Any divergence between the IEC recommendation and the corresponding national rules should, as far as possible, be clearly indicated in the latter.

PREFACE

This standard has been prepared by Sub-Committee 60A: Sound Recording, of IEC Technical Committee No. 60: Recording.

The text of this standard is based on the following documents:

Six Months' Rule	Report on Voting
60A(CO)95	60A(CO)106

Full information on the voting for the approval of this standard can be found in the Voting Report indicated in the above table.

The following IEC publications are quoted in this standard:

Publications 767 (1983): Helical-scan video tape cassette system using 12.65 mm (0.5 in) magnetic tape on type beta format.

774 (1983): Helical-scan video tape cassette system using 12.65 mm (0.5 in) magnetic tape on type VHS.

AUDIO RECORDING – PCM ENCODER/DECODER SYSTEM

1. Scope

This standard applies to the reversible process achieved by the PCM encoder/decoder system that transforms two audio signals into one PCM signal for compatibility with either the 60 fields/525 lines or the 50 fields/625 lines television system.

2. Object

This standard has been prepared to establish the signal format and other conditions required for the PCM encoder/decoder system that is intended for recording and reproducing audio signals in the form of a PCM signal through (part of) a domestic videocassette system. The standard seeks to achieve standardized system operation, compatibility of encoder/decoder systems with players and systems, and interchangeability of recorded tapes.

SECTION ONE – GENERAL

3. System description

The encoder of the PCM encoder/decoder transforms two audio signals into a PCM signal with redundant information added to correct occasional errors arising during recording or reproduction. The signal thus encoded is converted to a format that conforms to the relevant television system for recording on to a videocassette (see note).

The PCM signal is retrieved from the video signal by the videocassette system and most of the occasional errors are corrected by using the redundant information.

The decoder of the PCM encoder/decoder transforms the PCM signal into two audio signals.

Note. – Videocassette systems for household use are specified in IEC Publications 767 and 774.

SECTION TWO – FORMAT OF THE RECORDED SIGNAL

4. General

The format of the recorded signal shall be compatible with the signal of the relevant television system, either 60 fields/525 lines or 50 fields/625 lines.

5. **Transmission rate**

The transmission rate shall be as follows:

2.646 Mbit/s for the 60 fields/525 lines system;

2.625 Mbit/s for the 50 fields/625 lines system.

6. **Configuration of the synchronizing signal**

6.1 *Horizontal synchronizing signal*

The horizontal period containing the horizontal synchronizing signal shall be composed as shown in Figures 1a and 1b.

6.2 *Vertical synchronizing signal*

The vertical synchronizing signal with equalizing pulses shall be composed as shown in Figures 2a and 2b.

7. **Configuration of the horizontal line**

7.1 *Data synchronizing signal*

The data synchronizing signal shall consist of 4 bits as follows:

“ 1 0 1 0 ”

7.2 *Data block*

The data block shall consist of 128 bits and shall be NRZ (Non Return to Zero) modulated.

7.3 *White reference signal*

The white reference signal shall have a width of 4 bits and peak white level.

7.4 *Assignment in the horizontal period*

One horizontal period shall consist of 168 bits. The data synchronizing signal, the data block and the white reference signal shall be assigned into the horizontal period as shown in Figures 3a and 3b.

Each voltage level shall be measured when terminated by a 75 Ω load.

The tolerance of each level shall be $\pm 10\%$ (see Appendix A).

8. **Configuration of the vertical field**

8.1 *Audio data block line*

The audio data block line shall occupy the horizontal period containing the audio data block specified in Clause 11.

8.2 *Control data block line*

The control data block line shall occupy the horizontal period containing the control data block specified in Clause 12.

8.3 *Assignment in the vertical field*

Each field shall be headed by the vertical synchronizing signal with the equalizing pulse.

In the case of the 60 fields/525 lines system, as shown in Figure 4a, the control data block line shall be located at the 10th line for an odd field and 10.5th line for an even field.

The 245 audio data block lines shall follow the control data block line.

In the case of the 50 fields/625 lines system, as shown in Figure 4b, the control data block line shall be located at the 6th line for the first (third) field and 6.5th line for the second (fourth) field.

The 294 audio data block lines shall follow the control data block line.

The remaining lines in the field shall be left blank for both systems.

SECTION THREE – SOURCE ENCODING

9. Audio signal

9.1 Number of audio channels

The number of recorded audio channels shall be two, and shall be designated as A and B.

Channels A and B correspond to the left and right channels, respectively, for stereophonic use.

9.2 Emphasis

Pre-emphasis may be performed on the audio signal.

In that case, the time constants t_1 and t_2 shall be as follows:

$$t_1 = 50 \mu\text{s} \qquad t_2 = 15 \mu\text{s}$$

The characteristics of the pre-emphasis and de-emphasis are shown in Figure 5.

10. Source encoding

10.1 Sampling

The sampling rate shall be $44.100 \text{ kHz} \pm 0.01\%$.

It is recommended that both channels be sampled simultaneously.

It is permissible that the two channels be sampled alternately in the sequence of channel A followed by channel B.

10.2 Quantization

The sampled signal shall be recorded with 14-bit or 16-bit linear encoding.

Note. – The main body of this standard describes 14-bit encoding. Appendix B describes 16-bit encoding.

10.3 Coding

Two's complement binary code shall be used.

A positive binary code shall represent a positive audio signal voltage.

SECTION FOUR – DATA BLOCK

11. Configuration of the audio data block

11.1 General

The audio data block shall consist of six sampled signal words, two error correcting words and one error detecting word.

11.2 Sampled signal word

The sampled signal word shall consist of 14 bits with the MSB (Most Significant Bit) being bit 1 and the LSB (Least Significant Bit) being bit 14 as shown in Figure 6.

The nth sampled signal words for channels A and B are designated A_n and B_n respectively.

11.3 Error correcting word

Each of the error correcting words, designated P_n and Q_n , shall consist of 14 bits generated by the following equations (see Appendix B):

$$P_n = A_n + B_n + A_{n+1} + B_{n+1} + A_{n+2} + B_{n+2}$$

$$Q_n = T^6 A_n + T^5 B_n + T^4 A_{n+1} + T^3 B_{n+1} + T^2 A_{n+2} + T B_{n+2}$$

where: n is 0 or a multiple of 3

T is a generating matrix

Calculations shall be performed modulo 2.

The generating matrix T shall be defined as follows:

$$T = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{pmatrix}$$

The sampled signal words, A_n and B_n are expressed in the following column matrix:

$$A_n, B_n = \begin{pmatrix} \text{bit 14} \\ \text{bit 13} \\ \text{bit 12} \\ \text{bit 11} \\ \text{bit 10} \\ \text{bit 9} \\ \text{bit 8} \\ \text{bit 7} \\ \text{bit 6} \\ \text{bit 5} \\ \text{bit 4} \\ \text{bit 3} \\ \text{bit 2} \\ \text{bit 1} \end{pmatrix}$$

11.4 Interleaving

The eight word sequence consisting of six sampled signal words and two error correcting words is as follows:

$$[A_n, B_n, A_{n+1}, B_{n+1}, A_{n+2}, B_{n+2}, P_n, Q_n]$$

Interleaving of distance D shall be performed on the above sequence. As a result of the interleaving, the interleaved eight word sequence is shown as follows:

$$[A_n, B_{n-3D}, A_{n+1-6D}, B_{n+1-9D}, A_{n+2-12D}, B_{n+2-15D}, P_{n-18D}, Q_{n-21D}]$$

The distance D shall be equal to 16, which corresponds to 48 words.

11.5 Error detecting word

The error detecting word, designated CRC, consists of 16 bits generated by the following method.

“1”s shall be added, modulo 2, to each of the first 16 bits of the interleaved eight word sequence (112 bits).

After addition, each bit of the sequence corresponds to the coefficients of a polynomial having terms from X^{127} down to X^{16} .

This polynomial is divided, modulo 2, by the following generating polynomial:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The error detecting word is given by the coefficients of the terms from X^{15} to X^0 in the remainder polynomial resulting from the completion of this division.

Note. – The CRC is expressed as follows:

$$\begin{aligned} \text{CRC} = & (1 + b_1) X^{127} + (1 + b_2) X^{126} + \dots + (1 + b_{16}) X^{112} \\ & + b_{17} X^{111} + b_{18} X^{110} + \dots + b_{112} X^{16} \text{ mod } G(X) \end{aligned}$$

where: b_1 is the most significant bit of A_n and
 b_{112} is the least significant bit of Q_{n-21D} .

11.6 *Assignment in the audio data block*

Each word shall be assigned in the order: sampled signal words, error correcting words and error detecting word in one data block as shown in Figure 7.

12. **Configuration of the control data block**

12.1 *General*

The control data block shall consist of a cueing word, a content identification word, an address word, a control word and an error detecting word.

12.2 *Cueing word*

The cueing word shall consist of 56 bits as follows:

“ 110011001100 . . . 1100 ”

12.3 *Content identification word*

The content identification word shall consist of 14 bits. In this standard it shall be all 0s.

12.4 *Address word*

The address word shall consist of 28 bits and shall be divided into three separate codes: an index code, a time code and a field code.

Each code shall be expressed as a binary number.

12.4.1 *Index code*

The index code shall consist of 6 bits within the range of “000000 (00)” through “111111 (3F)”.

The updating of the index code shall be controlled at recording time.

12.4.2 *Time code*

The time code shall consist of 16 bits and shall be divided into “hour”, “minute” and “second”.

- The “hour” shall consist of 4 bits.
- The “minute” shall consist of 6 bits and shall be carried to the “hour” at every 60th count.
- The “second” shall consist of 6 bits and shall be carried to the “minute” at every 60th count.

The values of the “hour”, the “minute” and the “second” shall be reset by the control at recording time to zero or to preset values.

12.4.3 *Field code*

The field code shall consist of 6 bits and shall be carried at every 60th count for the 60 fields/525 lines system and at every 50th count for the 50 fields/625 lines system, respectively.

The value of the field code shall be counted at every field specified in Clause 8.

Odd and even numbers shall be assigned to odd and even fields, respectively.

The field code shall be reset by the control at recording time.

12.4.4 *Code assignment in the address word*

The index code, the time code and the field code shall be assigned within the address word, as shown in Figure 8.

Each code shall be laid out so that the MSB comes first and the LSB comes last.

12.5 *Control word*

The control word shall consist of 14 bits as shown in Table I.

12.6 *Error detecting word*

The error detecting word, designated CRC, shall consist of 16 bits and shall be generated from the 112-bit sequence of the cueing word, the content identification word, the address word and the control word in conformity with the specifications of Sub-clause 11.5.

12.7 *Assignment in the control data block*

Each word shall be assigned in the following order:

- cueing word,
- content identification word,
- address word,
- control word, and
- error detecting word (CRC)

as shown in Figure 9.

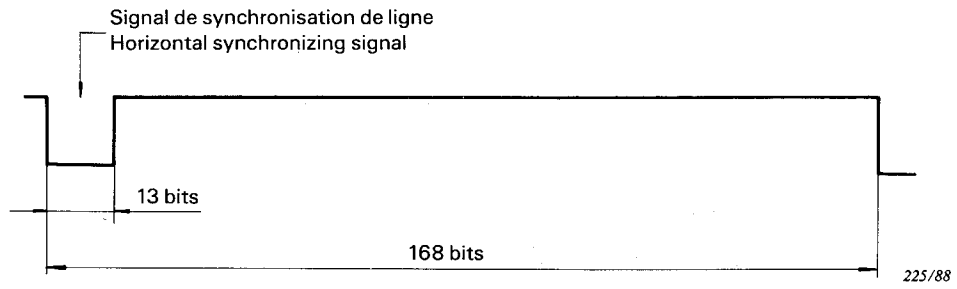


FIG. 1a. — Période de ligne (système à 60 trames/525 lignes).
Horizontal period (60 fields/525 lines).

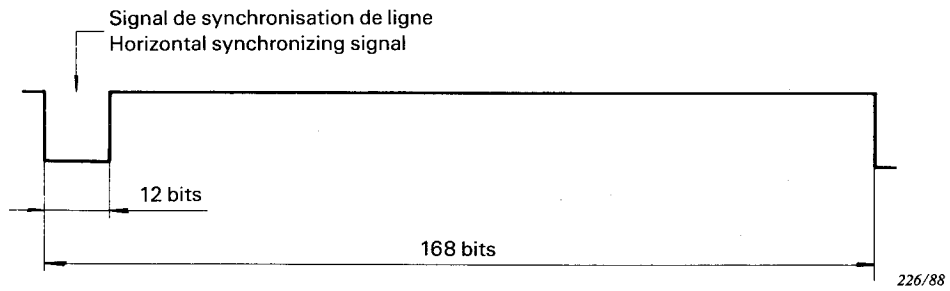


FIG. 1b. — Période de ligne (système à 50 trames/625 lignes).
Horizontal period (50 fields/625 lines).

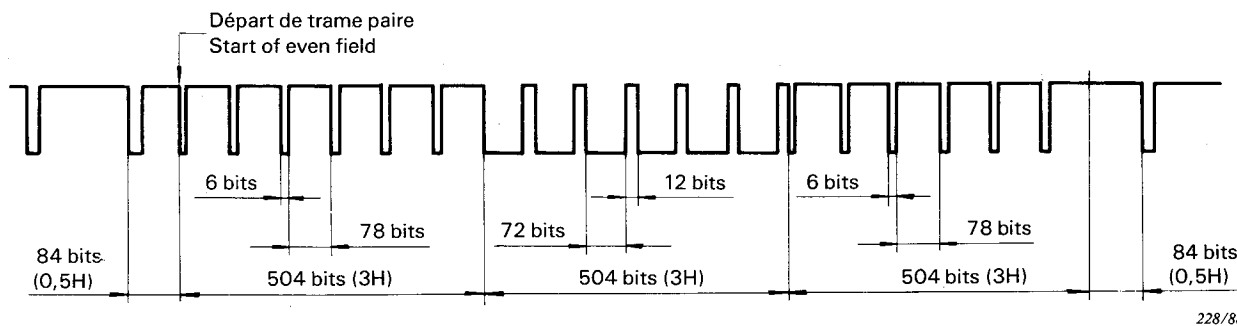
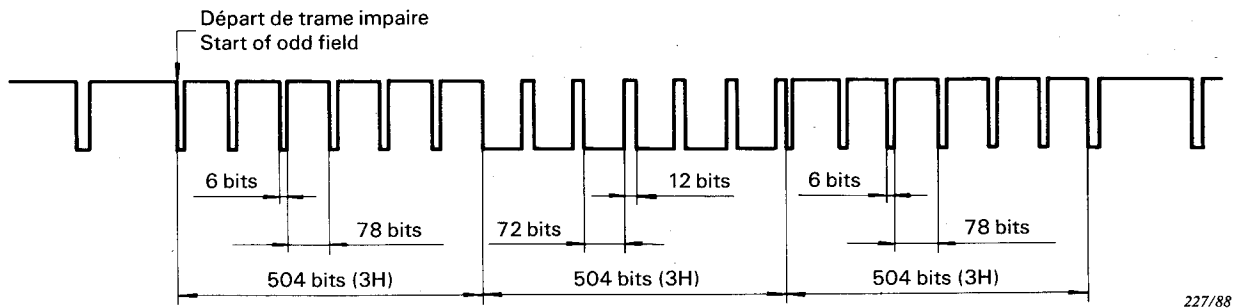


FIG. 2a. — Signal de synchronisation de trame (système à 60 trames/525 lignes).
Vertical synchronizing signal (60 fields/525 lines).

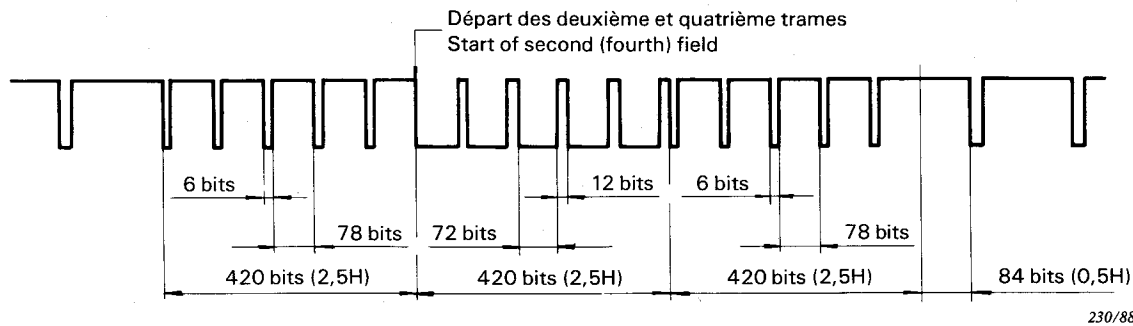
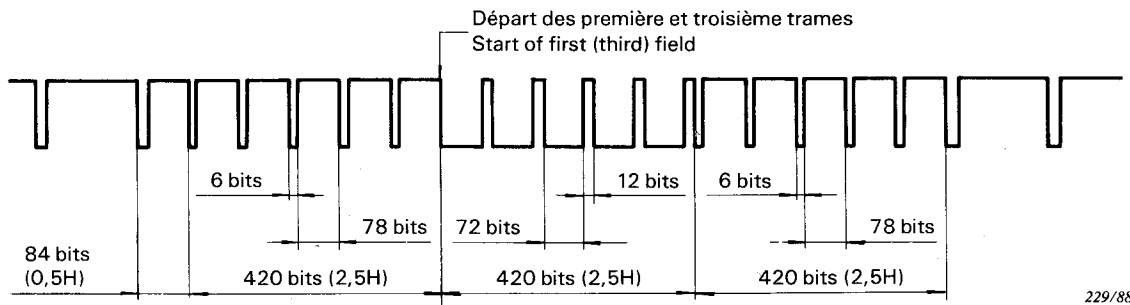


FIG. 2b. — Signal de synchronisation de trame (système à 50 trames/625 lignes).
Vertical synchronizing signal (50 fields/625 lines).

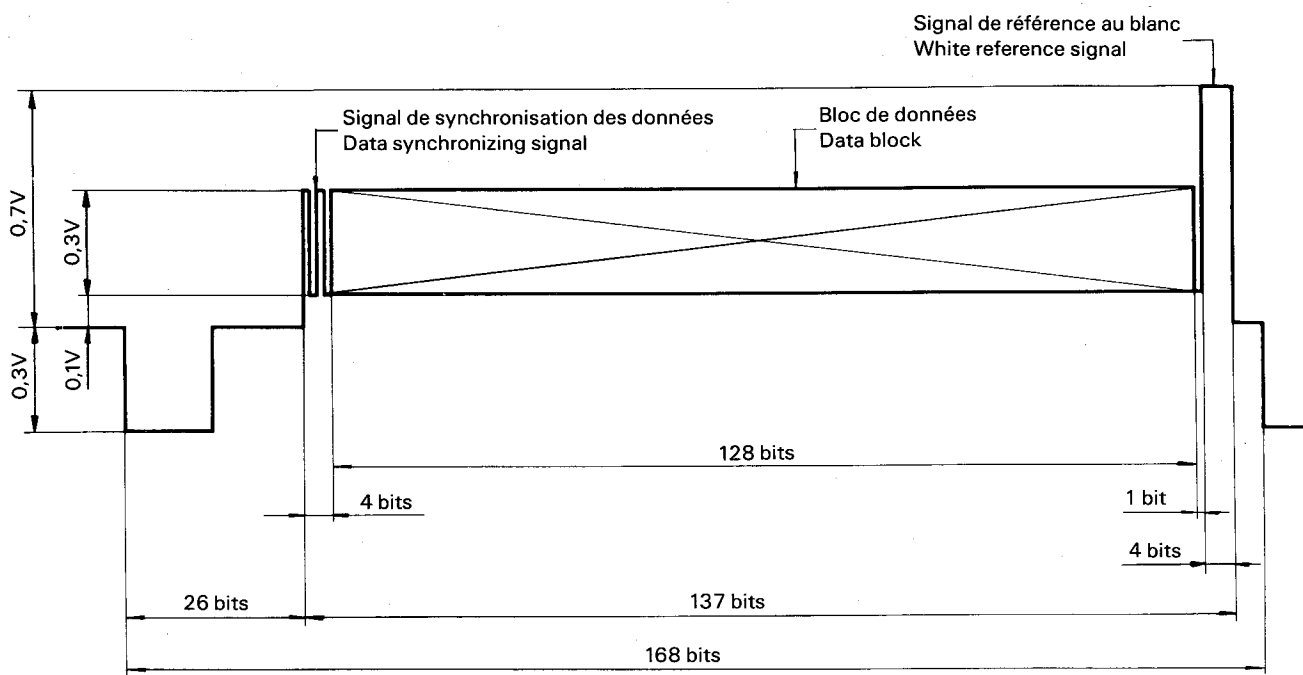


FIG. 3a. - Structure de la ligne (système à 60 trames/525 lignes).
Assignment in horizontal period (60 fields/525 lines).

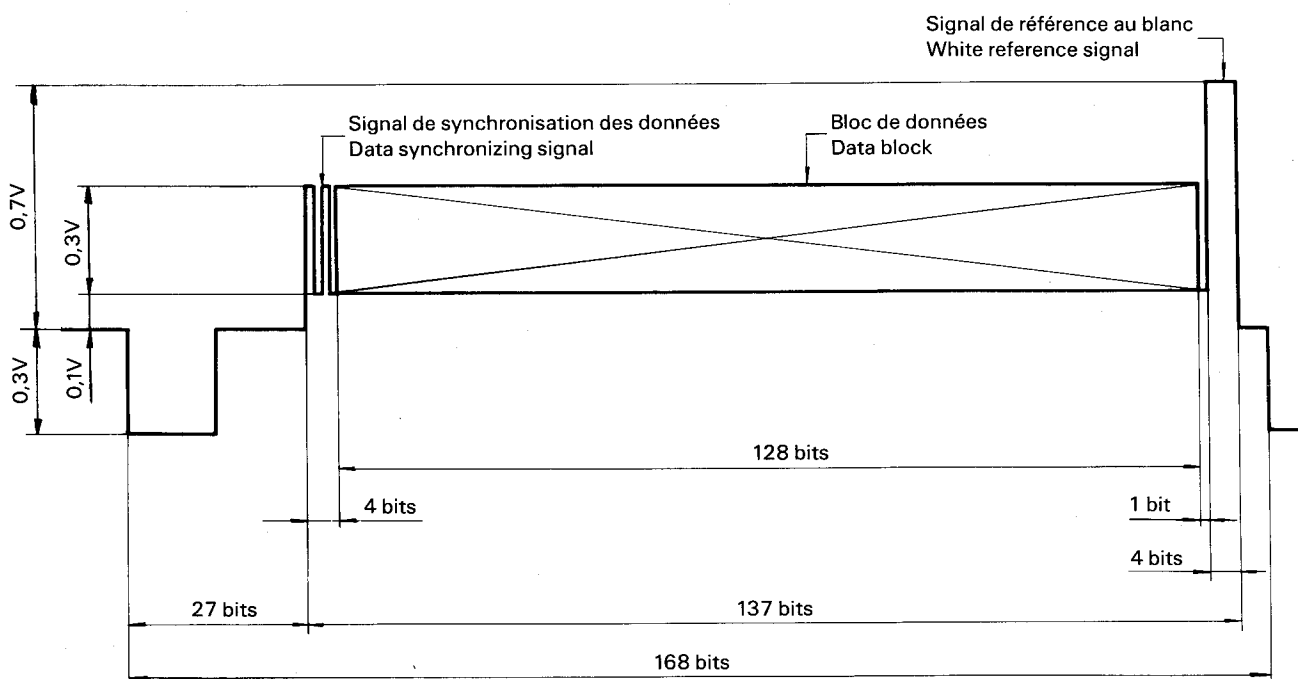
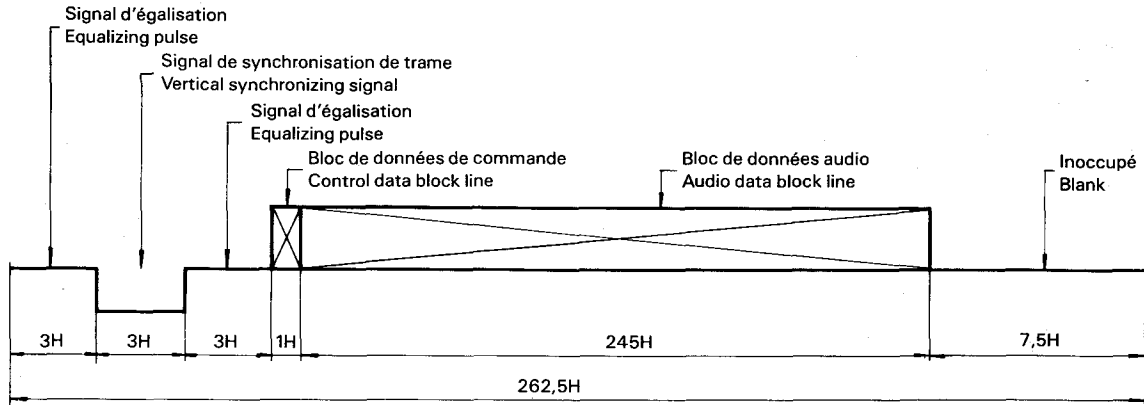


FIG. 3b. - Structure de la ligne (système à 50 trames/625 lignes).
Assignment in horizontal period (50 fields/625 lines).

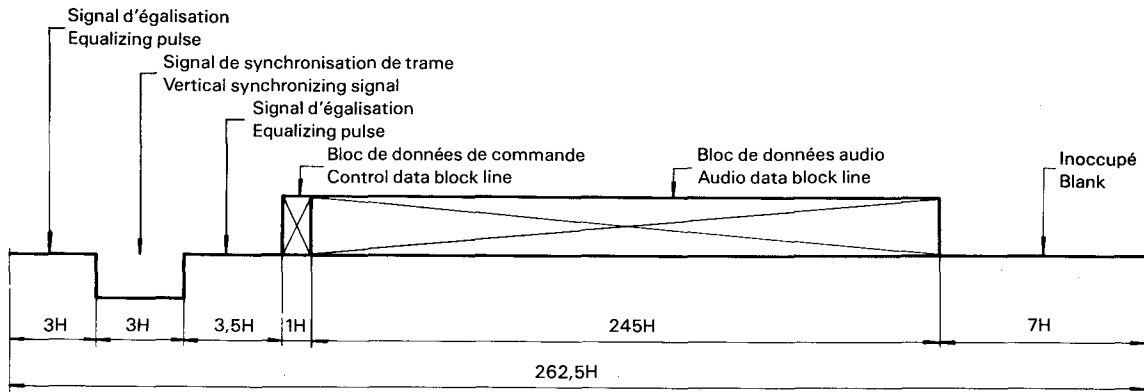
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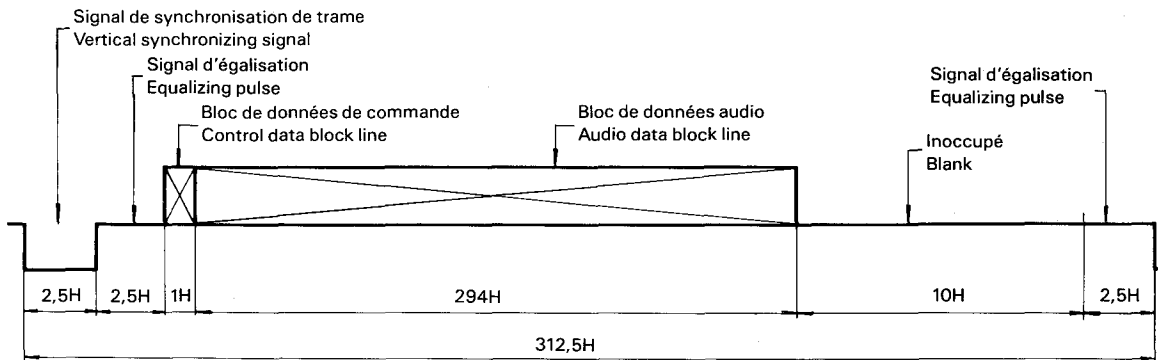


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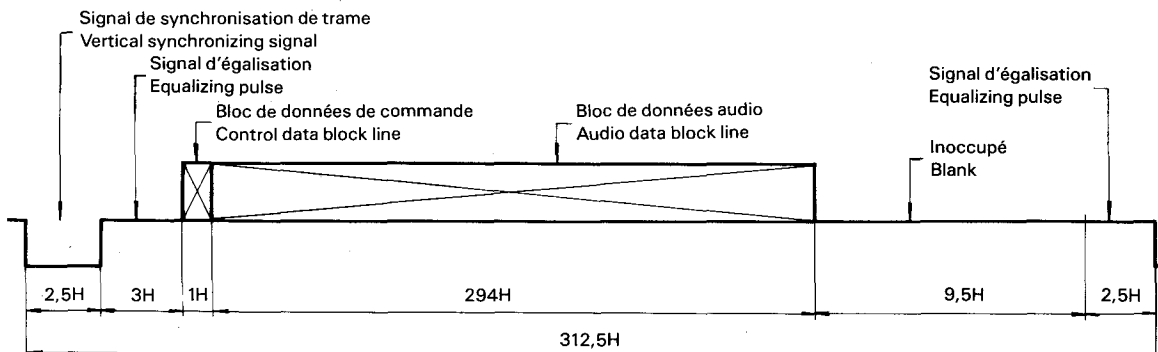


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FIG. 4a. - Structure de la trame (système à 60 trames/525 lignes).
Assignment in vertical fields (60 fields/525 lines).



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FIG. 4b. - Structure de la trame (système à 50 trames/625 lignes).
Assignment in vertical field (50 fields/625 lines).

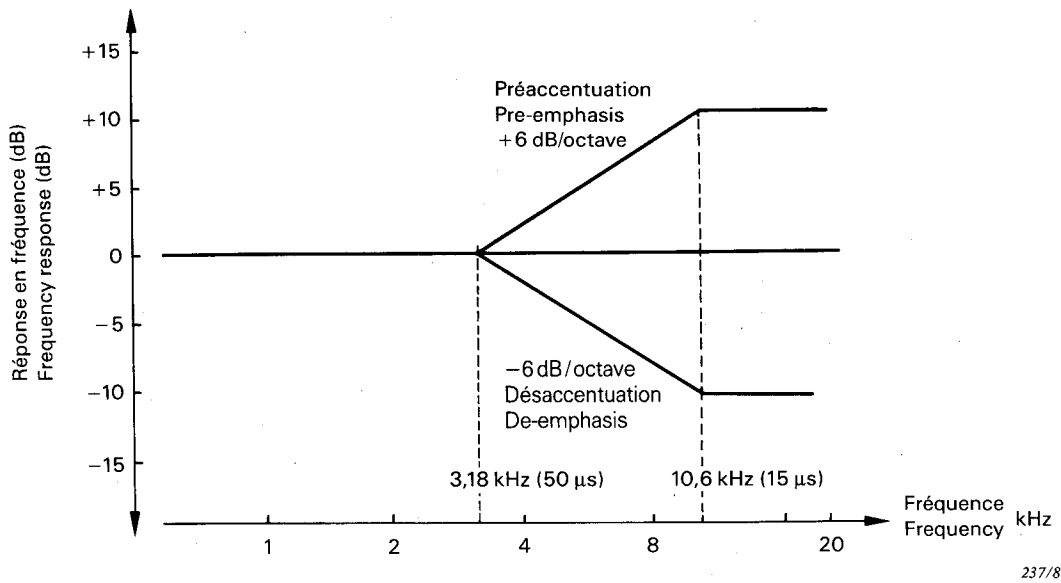


FIG. 5. — Préaccentuation et désaccentuation.
Pre-emphasis and de-emphasis.

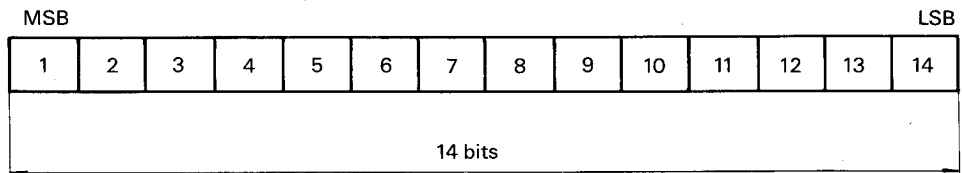


FIG. 6. — Mot d'échantillon de signal.
Sampled signal word.

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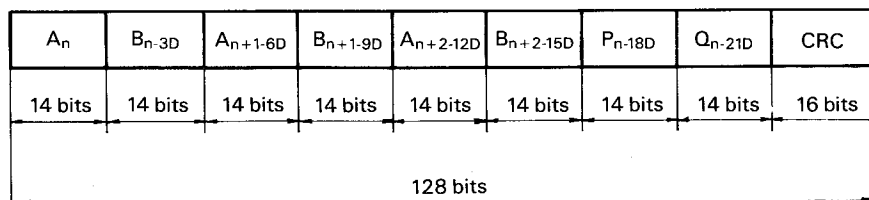
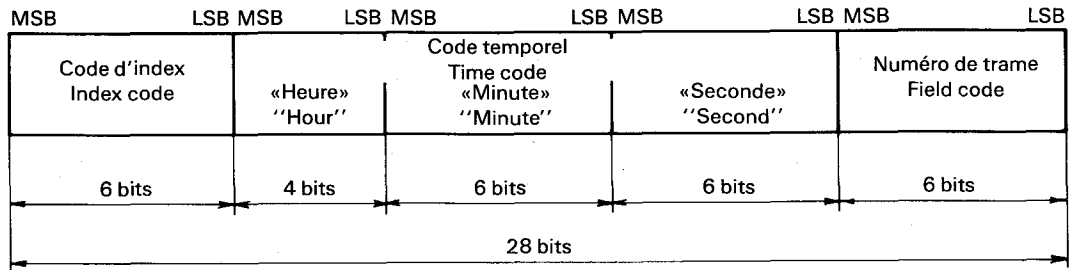


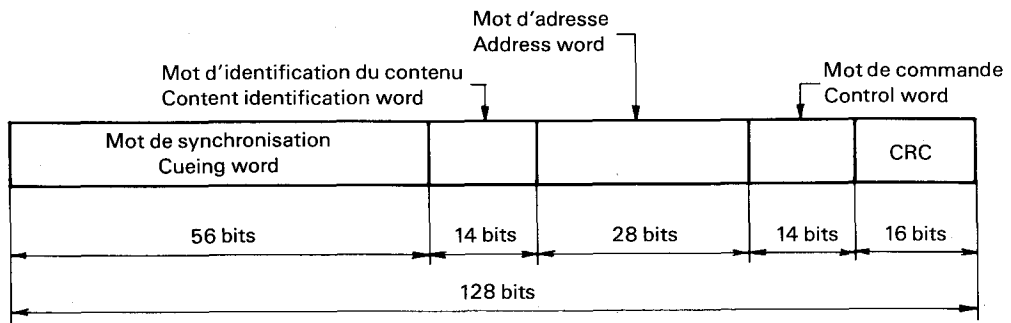
FIG. 7. — Structure du bloc de données audio.
Assignment in audio data block.

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FIG. 8. — Structure du mot d'adresse.
Assignment in address word.



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FIG. 9. — Structure du bloc de données de commande.
Assignment in control data block.

TABLE I
Status of control word

Bit No.	Content	Application	Code status
1- 2	Identification code conforming to this standard	By this standard	0 0
3-10	Not specified	-	0
11	Copy prohibiting code	Not prohibited	0
12	P-error-correction identification code	Applied	0
13	Q-error-correction identification code	Applied	0
14	Pre-emphasis identification code	Applied	0

APPENDIX A

NOISE LEVEL IN BACK PORCH

The noise level contained in the interval between the trailing edge of the horizontal synchronizing signal and the leading edge of the data synchronizing signal shall be 3 mV peak to peak, or less, on the PCM output terminals (terminated by a 75Ω load), in the band of 3579.5 ± 2 kHz, and 30 mV peak to peak, or less, in the band of 3579.5 ± 500 kHz for the 60 fields/525 lines system.

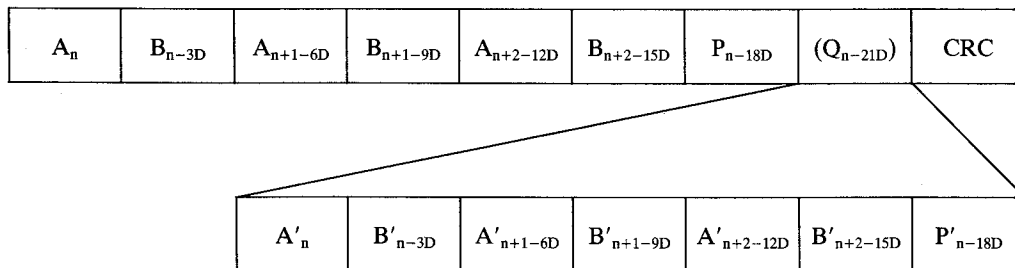
For the 50 fields/625 lines system, the noise level shall be 30 mV peak to peak, or less, in the band of $4.4 \text{ MHz} \pm 500 \text{ kHz}$.

APPENDIX B

ERROR CORRECTING WORD

1. As a general rule, both the error correcting words P and Q are applied.
2. In the 16 bit configuration, only the error correcting word P is applied.

Each of the last two bits of six sampled signal words and one error correcting word consisting of 16 bits shall be located at the position of the error correcting word " Q_{n-21D} " in the audio data block as shown in Figure B1.



A'_n, B'_n , etc., indicate the last two digits (in the order bit 15 and bit 16) of 16 bits.

FIG. B1. - Assignment in the audio data block.

APPENDIX C

VIDEO CASSETTE SYSTEM CONSIDERATIONS

For the adapter type encoder-decoder system, the following conditions should be met by the video cassette system to be connected.

1. Signal-to-noise ratio
Approximately 40 dB.
2. Jitter
Approximately 0.3%.
3. Skew
Approximately $\pm 15 \mu\text{s}$.
4. Output level
 $1 \pm 0.2 \text{ V}$ peak to peak.
5. Switching points
Some may be contained in the data.
6. Frequency characteristics
Frequency characteristics depend on the equipment.
7. Tracking
Manual adjustment may be required.
8. Tape conditions
Presence of creases and folds should be taken into consideration in the case of frequent use.

There are other unstable considerations for the output signal through the video cassette system, so that enough stability should be built in during design and manufacture.

For user convenience, it is desirable that the encoder-decoder system follow the variations as automatically as possible.

To adjust the tracking on the video cassette system, it is necessary to provide some means, such as an indicator, by which the optimum point can be determined.

Recently, more video cassette systems for domestic use are provided with the long-play mode in addition to the standard mode. In PCM recording, the standard mode is applicable from the viewpoint of stability and reliability.

The long-play mode is beyond the scope of this standard. However, a video cassette system with the long-play mode may have to be subjected to stricter PCM recording considerations, even if it is to be operated in the standard mode.

It is obvious that, in time, video cassette systems may be subjected to improvements in order to enhance the performance and functions of the original video recording equipment; hence, when designing PCM encoder/decoders, it is necessary to pay attention to technical trends.

It is also important to consider the design of video cassette systems in order to maintain their performance for PCM recording when combining video cassette and PCM encoder/decoder systems in accordance with this standard.

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